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[10191/2277]:

SEMICONDUCTOR ELEMENT AND METHOD OF MANUFACTURING THE SEMICONDUCTOR COMPONENT

Background Information

The present invention relates to a semiconductor component and a method of manufacturing same according to the definition of the species of the independent claims. German Patent Application 36 33 161 A1 describes a rectifier diode in which additional layout measures are provided in addition to a simple PN layer sequence to achieve an improved recovery behavior in commutation.

Advantages of the Invention

The arrangement according to the present invention and the method according to the present invention having the characterizing features of the independent claims have the advantage over the related art that they make it possible to provide semiconductor components having high clock frequencies and thus short switching times without requiring additional layout measures and without a steep drop in the clearing current in reversal of polarity to the reverse direction. This ensures in a simple manner that despite short switching times, no steep current chopping will result in high interference voltage peaks due to the omnipresent leakage inductance; it is thus readily possible to use rapidly switching components in motor vehicles for rectifier configurations in which such voltage peaks would otherwise interfere with radio reception, for example. In addition, the diode according to the present invention guarantees a low forward voltage in addition to the short switching time and a gentle drop in the clearing current, and thus it also ensures low heat losses in polarization of the voltage applied to the component in the forward direction.

Advantageous refinements of and improvements on the components and methods characterized in the independent claims are possible through the measures

characterized in the dependent claims.

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If the edge areas are formed by areas having no depressions, then the component is insensitive to damage and contaminants at the edge of the chip.

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Drawing

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Description of the Embodiments

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Figure 1 shows a diagram of a semiconductor diode having a weakly N-doped middle zone 2, which is covered with a strongly P-doped layer 1 on its top side and a strongly N-doped layer 3 on its bottom side. Layers 1 and 3 are provided with metallic coatings (not shown).

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Layers 1 and 2 form the PN junction of the semiconductor diode at their common interface.

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follows voltage curve 7, i.e., the positive half-wave of voltage curve 7 in the left half of the diagram. If the polarity of voltage 7 changes, the diode is polarized in the reverse direction but the current through the diode still approximately follows the voltage curve for a short period of time, called switching time 9, until developing into clearing current curve 8.

In switching from forward direction to reverse direction, charge carriers indicated into the middle zone must be cleared out before the diode is capable of receiving the reverse voltage. The time required for this is switching time 9.

The cross-sectional side view in Figure 3a shows a layer sequence 10, 20, 30 which forms a diode. Layer 10 is N-doped and corresponds to the doping of a weakly N-doped substrate used in the manufacture of this component. A highly N-doped layer 20 applied to the bottom side of layer 10 is in turn provided with a metallic coating (not shown) on its outside. A strongly P-doped layer 30 is applied to the top side of layer 10. Pits 60 defining first areas 40 and second areas 50 are introduced into the top side of the diode. In first areas 40, layer 10 is thicker than in second areas 50, while layer 30 has approximately the same thickness in both areas. Pits 60 are situated in internal area 70 of the diode, while the remaining area of the diode, the edge area, is formed by first areas 40. A metallic coating (not shown) is again applied to surface 80 of the diode. In the top view in Figure 3b, cross-section line 100 marks the location for which the cross-sectional side view is illustrated in Figure 1a. On surface 80 can be seen pits 60 formed parallel to the outside edges of the diode, with the pits intersecting and two parallel pits running parallel to each outside edge of the component. The depth of pits 60 is approx. 70 micrometers, for example, while the thickness of layer 10 in area 40 is approx. 80 micrometers and the thickness of layer 10 in area 50 is approx. 10 micrometers. Layers 20 and 30 are each approx. 60 micrometers thick. The doping concentration in layer 10 amounts to approx. $4 \times 10^{14} \text{ cm}^{-3}$, for example, and the doping concentration at the surfaces of layers 20 and 30 (the surface of layer 30 is labeled as 80 in Figure 3a) is approx. $7 \times 10^{19} \text{ cm}^{-3}$ each.

5 results in a short switching time and a low forward voltage of the semiconductor component according to the present invention. The edge area of the chip is formed by areas 40, so that the field strength at the edge of the chip remains low because of the higher breakdown voltage of areas 40 in comparison with areas 50. The diode is thus insensitive to damage and contaminants at the edge of the chip. If at least 25%
10 of the forward current of the diode is flowing through areas 40, then an extremely gentle current drop is guaranteed after reversal of polarity of the voltage to the reverse direction of the diode.

15 designed so that at least 50% of the current may flow through areas 50 to guarantee
at the same time a gentle current drop for a very low forward voltage. This may be
guaranteed through a corresponding number of pits or through a corresponding
choice of the width of the pits. In addition to square chips, pentagonal, hexagonal or
polygonal chips may be provided with the pits according to the present invention
20 arranged parallel to the respective edges of the chip and intersecting accordingly in
a pentagonal, hexagonal or polygonal pattern. The first type of conductivity is an N-
type line, and the second type of conductivity is a P-type line. Of course, the
selection may also be reversed. Semiconductor components other than diodes may
also be provided with the pits according to the present invention in an advantageous
25 manner. In particular in the case of diodes having three layers or four layers, i.e.,
transistor diodes or thyristor diodes, layers 30 and 10 then form the base-collector
layers or the P and N layers of the middle PN junction.

clock frequencies due to their short switching times. Therefore, they are suitable in particular for use in automotive bridge rectifier configurations in which clock

frequencies which are definitely above the frequencies of normal passive diode rectifiers are used. In the case of clocked rectifiers such as those described in German Patent Application 198 45 569.0, which was not published prior to the present application, clock frequencies of approx. 20 kHz may be achieved with the semiconductor diodes described here having pits, which is approximately one order of magnitude higher than the conventional frequency of known automotive rectifier configurations, which is linked to the rate of rotation of the alternator and amounts to a maximum of approx. 2 kHz.

To manufacture a diode chip according to Figure 3, parallel pits 60 are first cut in a wafer having the doping of subsequent layer 10. Then strongly P-doped and strongly N-doped layers 30 and 20, respectively, are diffused into this wafer simultaneously. In another step, a metal layer is deposited on both sides of the wafer. The wafer is then divided into individual chips by cutting in another step, with the dividing lines running in areas 40 where middle zone 10 is thick in comparison with areas 50 where pits 60 have been produced. This chip may be soldered into known press-fit diode housing and sheathed with epoxy resin, for example.

To obtain largest possible areas 50, it is advantageous to cut the pits with rectangular profiles. The number of pits per chip is also determined from the fixed area proportions of area 40 to area 50 and from the selected pit width.

The method according to the present invention provides such components without additional diffusion layers and without additional layout measures. This is a method which is suitable for mass production and is also suitable for implementation outside of the clean room to some extent, at least with regard to producing the pits.